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Description

Synchronous integrated memory

The invention relates to a synchronous integrated memory which outputs data to be read out, in synchronism with an external clock, at a data connection.

In synchronous DRAMs (Dynamic Random Access Memories), it is known for an internal clock to be produced within the memory from the external clock by means of a control unit in the form of a Delay Locked Loop (DLL), which internal clock leads the external clock and by means of which an output circuit of the memory is actuated. The output circuit outputs the data at the data connection with a phase shift with respect to the internal clock, and this phase shift corresponds to the phase shift between the internal clock and the external clock. The data are thus output at the data connection, synchronized to the external clock. After application of an external read command, the data are in this case intended to be present at the data connection within a specific number of clock cycles of the external clock. The predetermined number of clock cycles is also referred to as the "latency".

The invention is based on the object of specifying a synchronous integrated memory of said type, in which data to be read out are output at a data connection after a predetermined number of clock cycles of an external clock, once an output control signal has indicated the start of a read-out process.

This object is achieved by a synchronous memory as claimed in claim 1. Advantageous refinements and developments of the invention are the subject matter of the dependent claims.

The memory according to the invention has a control unit for producing a first internal clock, which leads the external clock by a specific phase shift. Furthermore, it has an output circuit which can be activated via an activation signal and which, in the activated state, starts an output process for the data to be read out, in synchronism with the first internal clock, and which outputs the data with the specific phase shift with respect to the first internal clock, that is to say in synchronism with the external clock, at the data connection. Furthermore, it has a clock generator for producing a second internal clock, which is synchronized to the external clock. The memory also has a counting unit, which starts a counting process for recording the number of successively following first levels of the first internal clock as soon as the second internal clock for the first time

assumes a first level while an output control signal is at a first level, and which activates the output circuit via the activation signal as soon as the number of successively following first levels of the first internal clock has reached a predetermined value.

The invention ensures that the data at the data connection are output delayed by the predetermined number of clock cycles of the external clock after the occurrence of the first level of the output control signal, since the first internal clock, whose first levels are counted by the counting unit, differs from the external clock only by the specific phase shift.

According to one development of the invention, the counting unit is supplied with a variable control signal via which different predetermined values can be set for the number of successively following first levels of the first internal clock. This allows the data which are to be read out to be output with adjustable latency.

According to one development of the invention, the counting unit has a shift register with a series circuit of register elements. One input of the first register element of the series circuit is supplied with the output control signal.

The first register element has a clock input to which the second internal clock is supplied, and the other register elements have clock inputs to which the first internal clock is supplied. Furthermore, the memory has a multiplexer via which the outputs of at least some of the register elements are connected to the activation input of the output circuit and whose switching state can be set via the control signal.

Since the register elements of the shift register operate in synchronism with the first internal clock, the multiplexer output signal which is supplied to the activation input of the output circuit is likewise synchronized to the first clock, by means of which the output process for the data to be read out is also started by the output circuit. The start of the output process, which is possible only when the output circuit is activated, thus takes place without any delay, synchronized to the first internal clock.

According to one development of the invention, the clock generator produces the second internal clock from the first internal clock, by means of a delay element. This can be done without any problems since the first internal clock leads the external clock by the specific phase shift.

According to one development of the invention, the control unit of the memory has an input which is connected to the

external clock and an output to which the input is connected via a variable delay unit and at which it produces the first internal clock. Furthermore, the control unit has a phase comparator with a first input which is connected to the input of the control unit, with a second input to which the output of the control unit is connected via the delay element of the clock generator, and with an output which is connected to a control input of the delay unit. In this development, the control unit is thus a Delay Locked Loop, in whose feedback path the delay element is arranged, and this delay element carries out two functions at the same time: firstly the setting of the specific phase shift between the first internal clock and the external clock. Secondly the generation of the second internal clock from the first internal clock. This double function of the delay element allows the memory to be constructed with fewer components than if the clock generator were to be constructed with components provided in addition to the components of the control unit.

The invention will be explained in more detail in the following text with reference to the figures, in which:

Figure 1 shows an output circuit and a counting unit of one exemplary embodiment of the synchronous memory,

Figure 2 shows a control unit of the synchronous memory, and

Figures 3 and 4 show various examples of signal profiles for the exemplary embodiment shown in Figures 1 and 2.

The synchronous memory shown by way of example here is a synchronous DRAM. Figure 1 shows a memory cell field MC of the memory, from which data D to be read out are output via an output circuit OUT to a data connection P. The output circuit has registers R and drivers DRV, which are not shown in any more detail. Furthermore, it has an AND gate AND, whose first input is a clock input for a first internal clock CLKI1, and whose second input is an activation input AKT. The output of the data D to be read out, by the output circuit OUT, depends on the output signal of the AND gate AND. In this case, the output circuit OUT has a delay ΔTOUT between the occurrence of a positive edge (which activates the output circuit) of the first internal clock CLKI1 at the first input of the AND gate AND with a high level at the same time at the activation input AKT, and the time at which a data item D to be read out is present at the data connection P.

According to Figure 1, the memory has a counting unit CT which comprises a shift register with register elements RE. By way of example, four register elements RE are shown, but this number may also assume other values in other exemplary embodiments of the invention.

One input I of each register element RE is connected to an output O of the preceding register element. The input I of the first register element RE of the series circuit is connected to an internal output control signal PAR, which is derived from an external read command which is supplied to the memory. Each register element RE has a clock input, with the clock input of the first register element being negative-level sensitive, the clock input of the second register element being positive-level sensitive, and the clock inputs of the other register elements being positive-edge sensitive. The clock input of the first register element RE is supplied with a second internal clock signal CLKI2, which is synchronized to an external clock CLKE which is supplied to the memory. The clock input of the first register element RE reacts to negative levels of the second internal clock CLKI2. The clock inputs of the other register elements RE are supplied with the first internal clock CLKI1.

According to Figure 1, the memory also has a clock generator G, which produces the second internal clock CLKI2 from the first internal clock CLKI1. This is done by means of a delay element, which has a delay time $\Delta TOUT'$, which corresponds as exactly as possible to the delay $\Delta TOUT$ of the output circuit.

The outputs O of the register elements RE, with the exception of the first register element, are connected via a multiplexer MUX to the second input of the AND gate AND. A control signal L which is supplied to the multiplexer MUX can be used to choose the register element output to which the activation input AKT of the output circuit OUT is conductively connected.

Figure 2 shows a control unit of the memory according to the invention in the form of a Delay Locked Loop (DLL), by means of which the first internal clock CLKI1 is produced from the external clock CLKE. The control unit CTR has an input to which the external clock CLKE is supplied, delayed by an input delay ΔTIN (which is caused by corresponding input circuits 1 of the memory), as a third internal clock CLKI3. The input of the control unit CTR is connected via a variable delay unit DEL to the control unit output, at which it produces the first internal clock CLKI1. Furthermore, the control unit CTR has a phase comparator φ, whose first input is connected to the input of the control unit CTR and which has a second input, to which the output of the control unit CTR is connected via two delay elements 10, 11. The first delay element 10 has a delay time ΔTOUT', which corresponds as exactly as possible to the delay time ΔTOUT of the output circuit OUT in Figure 1. The second delay element 11 has a delay time ΔTIN', which corresponds as exactly as possible to the delay time ΔTIN of

the input circuit 1. A control output C of the phase comparator φ is connected to a control input of the variable delay unit DEL, via which its delay time is set.

The first internal clock CLKI1, which is produced by the control unit CTR in Figure 2, leads the third internal clock CLKI3 by the sum of the delay times ΔTOUT', ΔTIN' of the delay elements 10, 11. Since the delay time ΔTIN' of the second delay element 11 corresponds to the delay time ΔTIN of the input circuit 1, the first internal clock CLKI1 thus leads the external clock CLKE by the delay time ΔTOUT' of the first delay element 10.

Figure 2 shows a further exemplary embodiment of the invention, indicated by the dashed arrow, in which the output signal of the first delay element 10 is used as the second internal clock CLKI2. In this case, the first delay element 10 is a component of the clock generator G and is identical to the delay element shown in Figure 1. In the exemplary embodiment being considered here, the delay element of the clock generator G in Figure 1 is, however, present in addition to the first delay element 10 of the control unit CTR.

Since the second internal clock CLKI2 is produced from the first internal clock CLKI1 by the clock generator G with a

positive phase shift of ΔTOUT', it is synchronized to the external clock CLKE. In this case, "synchronized" means that the two clocks have virtually no phase shift with respect to one another.

Figures 3 and 4 show various examples of signal profiles of the external clock CLKE, of the output control signal PAR, of the internal clocks CLKI1, CLKI2, CLKI3 and of the data output at the data connection P. Figures 3 and 4 show signal profiles for various frequencies of the clock signals with a constant delay time ΔTOUT from the output circuit OUT. The scales in Figures 3 and 4 thus differ. It can be seen that the second internal clock CLKI2 is synchronized to the external clock CLKE, and the first internal clock CLKI1 leads the external clock CLKE by the delay time TOUT of the output circuit OUT. The output control signal PAR is synchronized to the third clock signal CLKI3 at the input of the control unit CTR from Figure 2.

For the signal profiles illustrated in Figures 3 and 4, the multiplexer MUX from Figure 1 is actuated via the control signal L such that it connects the output O of the penultimate register element RE to the activation input AKT of the output circuit OUT. This means that the memory has a latency of 2. This can best be explained with reference to the last line in

Figures 3 and 4: once an external read command CMD, which is supplied to the memory, has occurred, two and only two clock periods of the external clock CLKE must follow before the data to be output are actually present at the data connection P. This is indicated by the double arrows denoted by the numbers 1 and 2 in Figures 3 and 4.

The counting unit CT shown in Figure 1 ensures that the latency is maintained, in the following way: as soon as the output control signal PAR, which is derived from the external read command CMD, becomes active at a high level, it starts a counting process as soon as the second internal clock CLKI2 is at a negative level. The contents of the register elements RE are all set to zero in advance. The "one" (which is thus stored by the first register element RE) in the output control signal PAR is then accepted by the second register element RE as soon as the first internal clock CLKI1 is at a high level.

The subsequent register element RE each accept this "one" when a subsequent positive edge serves on the first internal clock CLKI1.

Thus, as soon as the output control signal PAR assumes a positive level and provided the second internal clock CLKI2 is at a low level, the counting unit CT from Figure 1 thus counts the subsequent positieve levels of the first internal clock

CLKI1. In this case, the output signal of the counting unit CT is synchronized to the first internal clock CLKI1, since the register elements RE are clocked by it.